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General Description

The AL1101 stereo ADC is a high performance 24-bit analog to digital audio converter. Dynamic range is 107dB (A-weighted). The sensible pinout and easy user interface are unprecedented. The part has an internal high quality phase-locked loop that eliminates the need for external high frequency clocks.

Features

- ❑ 24 bit conversion
- ❑ 107dB dynamic range (A-wt)
- ❑ .002% THD (input=-1dBFS)
- ❑ 64X oversampling, 5th order 1 bit Δ-Σ modulator
- ❑ 64:1 linear phase digital decimation filter
- ❑ sample rate variable from 24kHz to 55kHz
- ❑ digital high-pass filter
- ❑ total power consumption 110mW (Fs=48kHz)
- ❑ internal PLL derives all necessary timing signals from one external Fs clock
- ❑ serial output bit-rate selectable 32/24 bits/frame
- ❑ full scale differential input =+/-4V ([IN+]-[IN-])
- ❑ 5V operation

INL+ — 1	16 — INR+
INL-	INR-
AGND	MID
REF+	VA
REF-	AGND
VD	DGND
DGND	DOUT
FORMAT — 8	9 — WDCLK
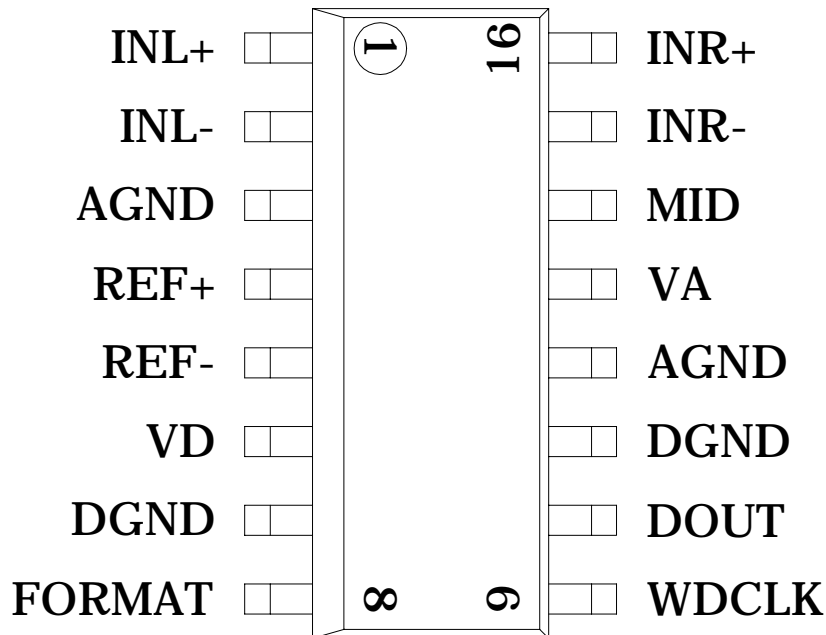
16 pin SOIC
150 mils wide

DS1101-1000

Pin Description

Pin #	Name	Pin Type	Description
1	INL+	INPUT	positive analog input, left channel
2	INL-	INPUT	negative analog input, left channel
3	AGND	GND	analog ground
4	REF+	PWR	pos reference, 5V thru 1K, connect .1μ bypass to REF-
5	REF-	GND	negative reference, connect to GND
6	VD	PWR	digital supply, 5V, connect .1μ bypass cap to GND
7	DGND	GND	digital ground
8	FORMAT	INPUT	format select, 0=32 bits/frame, 1=24bits/frame
9	WDCLK	INPUT	sample frequency wordclock, 24kHz<Fs<55kHz
10	DOUT	OUTPUT	serial data output
11	DGND	GND	digital ground
12	AGND	GND	analog ground
13	VA	PWR	analog supply, 5V, connect .1μ bypass cap to GND
14	MID	OUTPUT	mid reference, connect .1μ bypass cap to GND
15	INR-	INPUT	negative analog input, right channel
16	INR+	INPUT	positive analog input, right channel
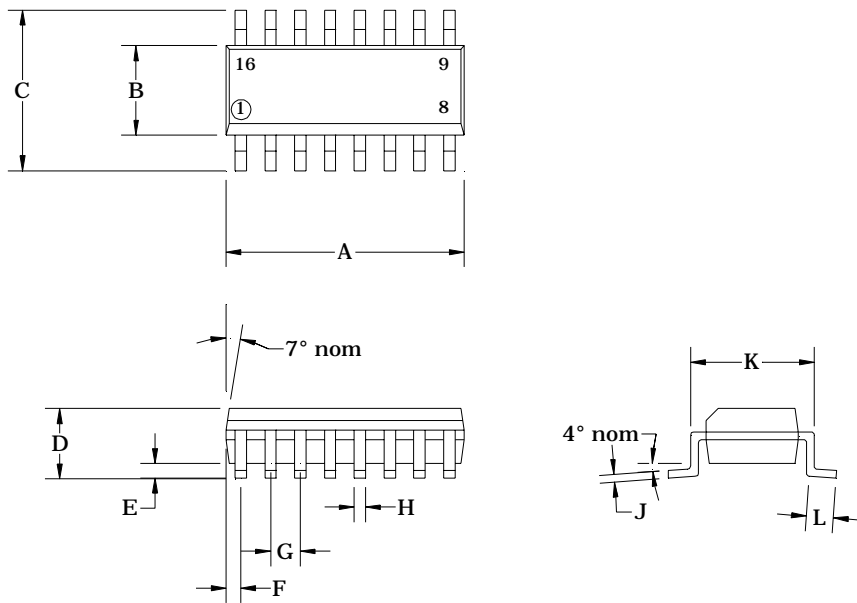
Dimensions (Typical)		
	Inches	Millimeters
A	.389"	9.88
B	.154"	3.91
C	.236"	5.99
D	.100"	2.50
E	.008"	0.20
F	.025"	0.64
G	.050"	1.27
H	.017"	0.42
J	.011"	0.27
K	.170"	4.32
L	.033"	0.83

Notes:

1) Dimension "A" does not include mold flash, protrusions or gate burrs.

Analog Characteristics

(Ta=25 C, VA=VD=V_{REF}=5V, Fs=48kHz, input freq=1kHz, measurement bandwidth=20Hz-20kHz, unless otherwise specified)

Parameter	Comments	Min	Typ	Max	Units
Dynamic Range	input=-60dBFS (A-wt)		107		dB
THD+N	input=-1dBFS		-95		dB
	input=-20dBFS		-84		dB
	input=-60dBFS		-44		dB
Crosstalk	input=-1dBFS		-130		dB
Input Voltage	[IN+]-[IN-] fullscale	+/-4.0		+/-4.2	V
	interchannel match		.01		dB
	common mode dc bias		2.5		V
Input impedance	differential		160k		Ohm
Power Supply Current	analog (I_A)		16		mA
	digital (I_D)		6		mA
REF current	$I_{REF}{}^2$		130		µA
Power Consumption			110		mW
Gain Error	REF+ held at 5V			+/-.34	%
PSRR	REF+ held at 5V		70		dB

Note 1: Full scale input scales linearly with REF potential ([REF+]-[REF-]).
Note 2: REF current scales linearly with Fs.

Digital Filter Characteristics

(Ta=25 C, VA=VD=V_{REF}=5V, Fs=48kHz)

Parameter	Comments	Min	Typ	Max	Units
Passband	-3dB bandwidth [1,2]	2.5		21.77K	Hz
	Ripple (20Hz-21.7kHz)			+/-.025	dB
Stopband	Frequency [1]	26.23k			Hz
	Attenuation	-76			dB
Group delay			37.9		1/Fs
Group delay distortion			0		µs
Highpass Filter	Fc [1]		2.5		Hz
	-0.1dB frequency		16.4		Hz

Note 1: passband, stopband, and highpass frequencies scale with Fs.
Note 2: passband is compensated for external single-pole 80kHz lowpass filter at
analog inputs (.26dB at 20kHz). Compensation scales with Fs.

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Recommended Operating Conditions
(GNDA=GNDD=0V)

Parameter	Comments	Min	Typ	Max	Units
VA	analog supply voltage	4.5	5.0	5.5	V
VD	digital supply voltage	4.5	5.0	5.5	V
T_a	ambient temperature	0	25	70	degC
Fs	sample frequency	24	48	55	kHz
C_{load}	DOUT load capacitance			30	pF

Electrical Characteristics – Digital Pins

Parameter	Comments	Min	Typ	Max	Units
INPUTS (WDCLK, FORMAT)					
V_{IH}	Logical "1" input voltage	0.55VD			V
V_{OH}	Logical "0" input voltage			.1VD	V
I_{IN}	input leakage current			1	µA
C_{IN}	input capacitance		5		pF
OUTPUTS (DOUT)					
V_{OH}	Logical "1" output voltage	0.9VD			V
V_{OL}	Logical "0" output voltage			0.1VD	
I_{OH}	Logical "1" output current		-0.5		mA
I_{OL}	Logical "0" output current		0.5		mA

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System Description

Serial Interface and Timing

The AL1101 presents its 2's complement serial data in a standard MSB-first format. Two bit-rates are provided. The 32-bits/frame rate (FORMAT low) is suitable for use in systems where 256 Fs master clocks are present. The 24-bits/frame rate (FORMAT high) is convenient when interfacing with circuits where 384 Fs master clocks are present.

The output sample period is defined between rising edges of wordclock (WDCLK) input. Nominally, this is a 50% duty-cycle clock at frequency Fs, but it can be a pulse with $Ts/256 <$ pulse-width $< Ts$ (255/256); $Ts=1/Fs$. Left channel data output starts when WDCLK rises and right channel data output starts Ts/2 seconds later (when WDCLK falls if 50% duty cycle).

The serial bits are output on the rising edge of an internally generated bit clock (rising edge aligned with rising edge of WDCLK) that runs at 64Fs when FORMAT is low (32 bits/frame), or 48Fs when FORMAT is high (24 bits/frame). The data is valid +/-100ns from the center of these bit-frames. See timing diagram on next page.

Input Logic Levels

The AL1101 can properly receive input logical '1' voltages of .55VD. This means the AL1101 can interface directly with logic signals supplied from 3.3V systems. No special interface circuitry is required.
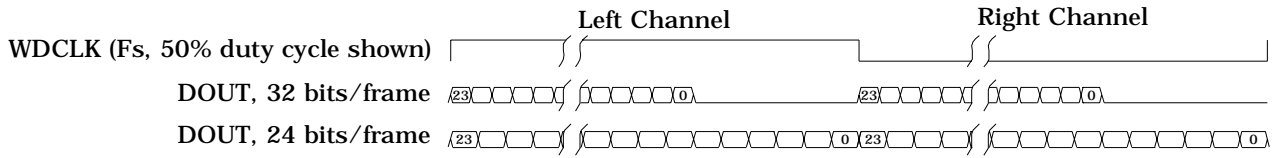
Internal Phase-Locked Loop (PLL)

The AL1101 contains an internal PLL that locks to the rising edge of WDCLK and produces all necessary high frequency clocks and timing signals to operate the device. This high quality PLL will reject any high-frequency jitter on the incoming wordclock (jitter rejection corner approx. 4kHz).

The PLL allows a simplified user interface and eliminates the need of running high frequency clocks on PCB traces to the part. This reduces unwanted RF noise and coupling problems that can occur when these clocks are required as input pins for a device.
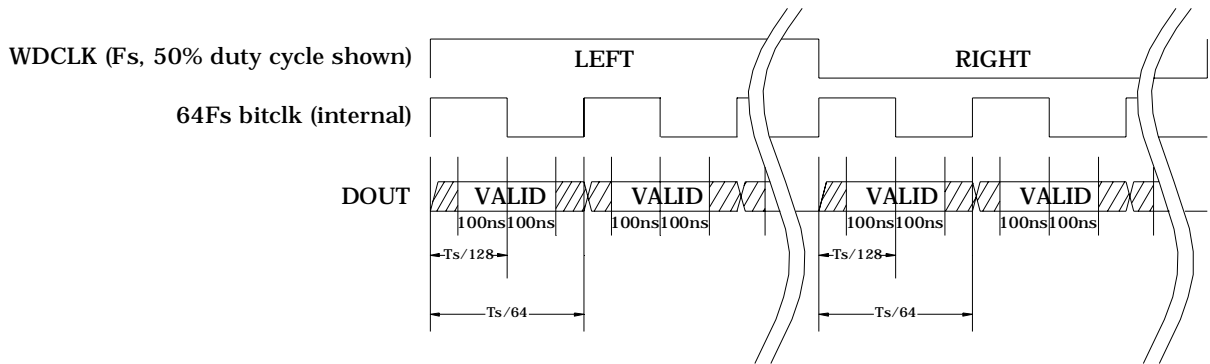
Digital High Pass

The AL1101 has an internal 2.5Hz single pole digital filter. The filter removes any offset present in the internal amplifiers and prevents DC codes from appearing at the data outputs. The response of the filter is -.067dB at 20Hz.

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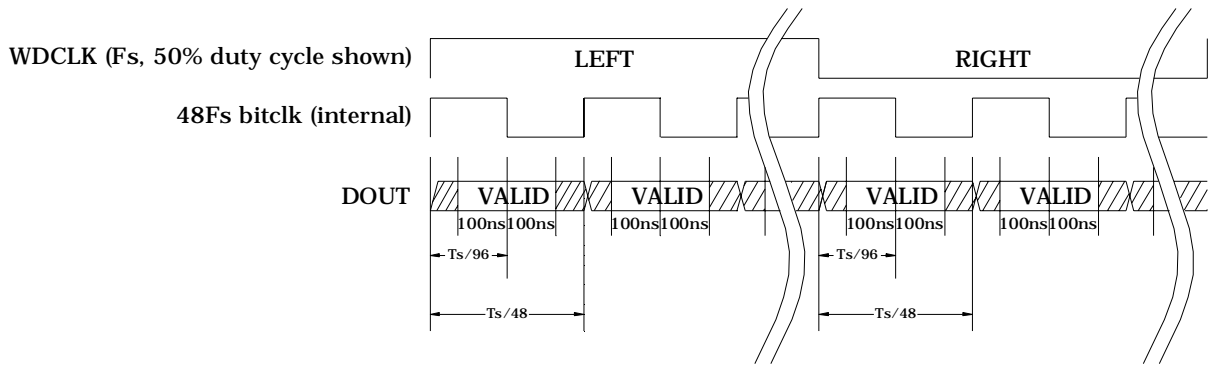Alesis Semiconductor
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Serial Outputs Formats

Left Channel   Right Channel

WDCLK (Fs, 50% duty cycle shown)

DOUT, 32 bits/frame   (23)⟍⟍⟍⟍⟍/ ⟍⟍⟍⟍⟍(0)   (23)⟍⟍⟍/ ⟍⟍⟍⟍(0)

DOUT, 24 bits/frame   (23)⟍⟍⟍/ ⟍⟍⟍⟍⟍⟍⟍⟍(0)(23)⟍⟍/ ⟍⟍⟍⟍⟍⟍⟍⟍⟍(0)

Timing Example

32 bits/frame

WDCLK (Fs, 50% duty cycle shown)   LEFT   RIGHT

64Fs bitclk (internal)

DOUT   /// VALID /// VALID /// /// VALID /// VALID ///
             100ns 100ns   100ns 100ns   100ns 100ns   100ns 100ns
        ←Ts/128→   ←Ts/128→

        ←——Ts/64——→   ←——Ts/64——→

24 bits/frame

WDCLK (Fs, 50% duty cycle shown)   LEFT   RIGHT

48Fs bitclk (internal)

DOUT   /// VALID /// VALID /// /// VALID /// VALID ///
             100ns 100ns   100ns 100ns   100ns 100ns   100ns 100ns
        ←Ts/96→   ←Ts/96→

        ←——Ts/48——→   ←——Ts/48——→

Analog Inputs

The AL1101 inputs are self-biased to MID potential. Input signals larger than maximum levels (+/-4V differential) and smaller than supplies are output limited to maximum positive and negative levels in the digital section (7fffffH and 800000H respectively).

The digital section of the AL1101 compensates for the passband amplitude deviation of an external single-pole 80kHz anti-alias filter (@ Fs=48k, scales with Fs). To remove high-frequency noise at the differential inputs, the capacitor between the differential inputs should be located as close as possible to the input pins.
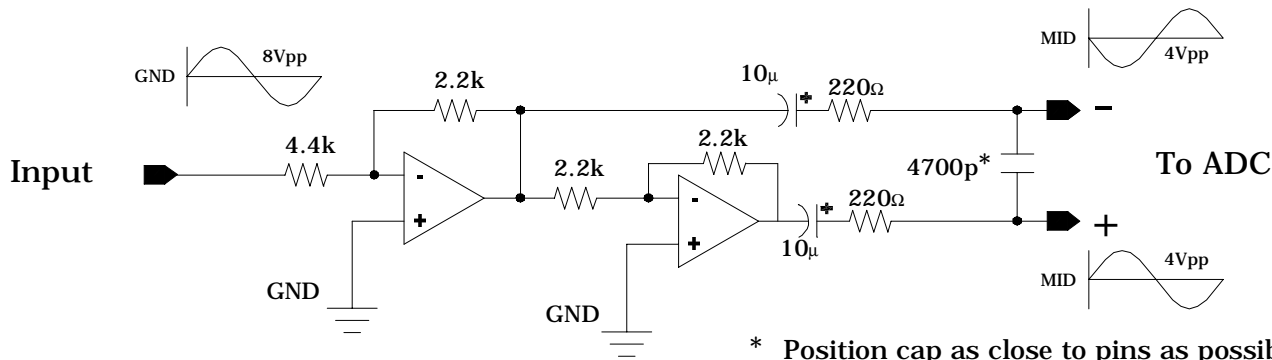
* Position cap as close to pins as possible. Film or high quality ceramic capacitor suggested.

**Input Conditioning Circuit**

Reference and MID

The differential potential between the REF+ and REF- pins (connected to 5V and GND respectively) determines the amount of charge that is added to or removed from the modulator's first stage during each input sample period (64Fs). It is very important that REF+ is well bypassed to REF- (.1μF ceramic as close as possible to pins) to remove the unwanted effects of high frequency noise.

The MID potential is developed on chip (VA/2 volts) and is used to bias the internal amplifiers in the modulator, and to provide a reference which determines the polarity of the modulator output. It requires a .1μF bypass to GND at the pin. No load current should be taken from the MID pin.

Power Supplies and Ground

A single low-impedance 5V supply is all that is required to achieve specified performance. A 5V supply plane is recommended if possible. VA and VD can be directly connected to 5V, and REF+ should be isolated with a 1k-ohm resistor to 5V.

A single low impedance ground plane can be used for all GND connections, simplifying PCB layout. Each supply pin should be bypassed to GND with a .1μF ceramic cap positioned as close to the pins as possible.
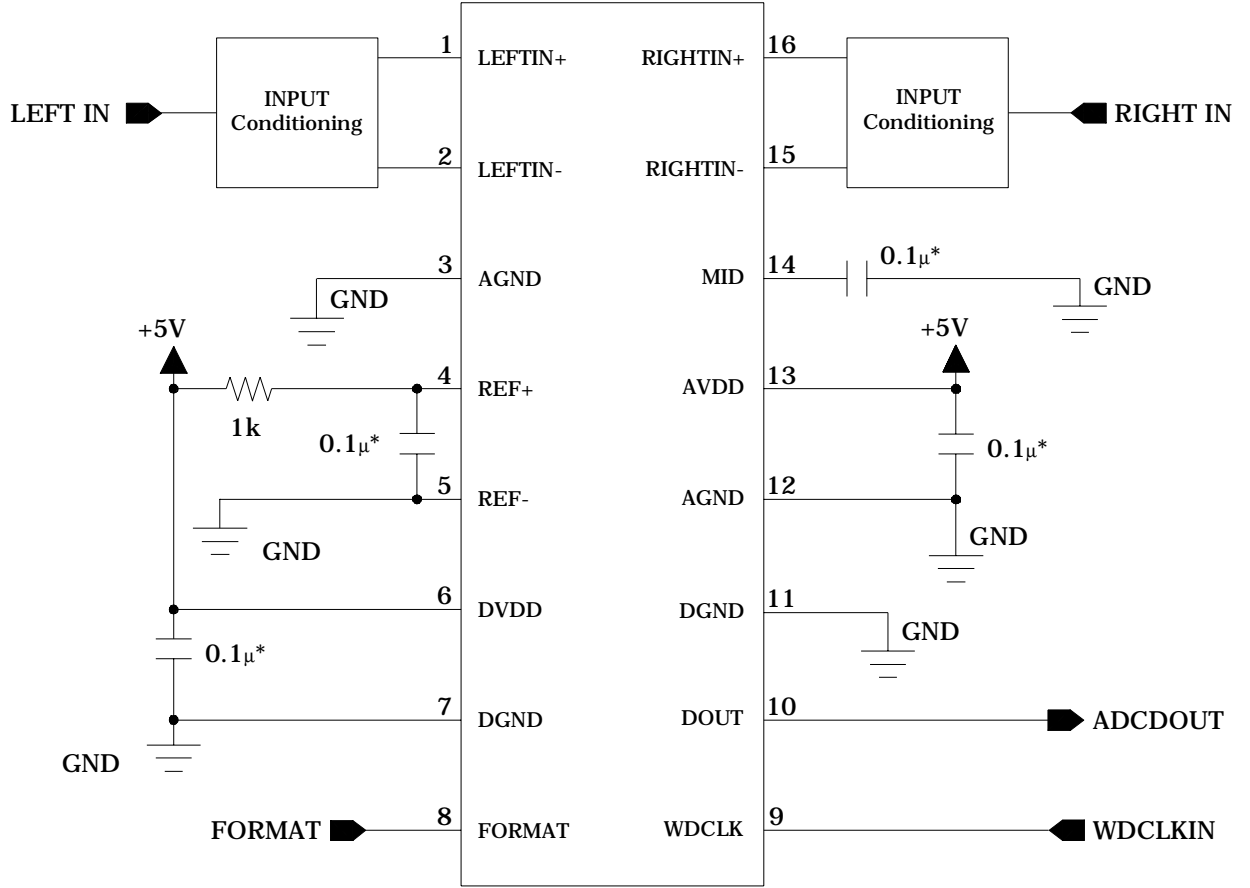
24-bit ADC
Suggested Connections

* Position caps as close to the pins as possible.

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